COMMUNICATION DEVICE AND METHOD HAVING

A COMMON PLATFORM

BACKGROUND

Technical Field

The present invention relates to a communication device and method; in particular, a communication device and method having a plurality of processors and applications which operate under a common platform.

Discussion of Related Art

Recent advances in semiconductor, wireless, and software technologies make available a multitude of applications operable from mobile communication devices such as cellular phones and PDAs. For example, handheld phones used for wireless communication are also usable as PDAs, cameras, game play devices, etc. These applications were available previously as separate standalone devices. In these multi-application communication devices, there are usually at least two integrated circuit chips, each with one or more processing devices. One of the two chips serves as a modulator/demodulator ("modem"). The modem chip includes a digital signal processor ("DSP") for signal processing purposes to effect wireless communications with base stations or other communication devices. The other chip is an application processor ("AP"),

having a central processing unit ("CPU") to operate functions and peripherals such as camera or image capture, display, 2D/3D engine/memory, database, etc. Because each application or peripheral operates with a different platform, the CPU communicates with each of the applications and peripherals through

5   interfaces which are distinct and specific to the respective application. The different interfaces are usually embedded within the AP chip. Each of the AP and modem chips in the communication device has respective local memory for data and program storage, controlled by its respective processor. Each of the AP and modem chips also runs its respective operating system or platform.

10   Communications between the AP and the modem chips are made through a shared memory and respective interfaces.

Figure 1 shows a simplified block diagram of a conventional communication device having the above described configuration, with a modem chip and an application processor chip for operating application or peripheral

15   devices such as a camera, an LCD display, RAM and ROM. A dual-port SRAM serves as the shared memory for facilitating communication between the AP and modem chips. Each chip has its respective memory controllers for controlling the local RAM and ROM and the shared memory.

Figure 2 shows a more detailed block diagram of the conventional

20   communication device of Figure 1. As shown, the AP chip 110 includes a CPU 111 for controlling peripheral devices such as LCD module 120, camera module 130, and memory module 140. Because each application/peripheral has its own operating system, there must be separate interfaces or control units for

respective applications, such as LCDC 113 for controlling the LCD module 120, CAM controller 115 for controlling the camera module 130, and memory controller 117 for controlling memory module 140. Further, each application connects to the AP chip 110 through different buses at different pinouts of the

5   chip. As an example, the LCD module 120 requires a 30-pin bus connection to the LCDC 113, the camera module 130 requires a 20-pin bus connection to camera control unit 115, and the memory module 140 requires a 50-pin bus connection to memory controller 117.

The modem chip 150 includes a DSP 155 and coprocessor 151 for

10   effecting radio communication functions. The DSP 155 communicates with coprocessor 151 through internal interface 153. The modem chip 150 connects to an external memory module 160 via a memory controller 157. Communication between the AP chip 110 and modem chip 150 is by interface line 170, via a shared memory (not shown). Individual memory controllers 119 and 159 are

15   disposed within respective AP chips 110 and modem chip 150 to independently access through respective ports of the dual port shared memory.

In mobile devices such as a cellular phone with multiple applications such as that shown in Figs. 1 and 2, the physical size of the AP chip 110 is comparatively large because of the requirement for the large number of pinouts

20   and the different busses and interfaces. Also, operation of multiple applications with different platforms requires constant processing by the CPU 111, therefore, power consumption would be relatively high.

3

A need therefore exists for a mobile communication device and method having multiple applications which minimizes physical size and power consumption.

SUMMARY OF THE INVENTION

According to an aspect of the present invention, a communication device is provided, comprising: a signal modulator/demodulator having a digital signal processor for effecting radio communications; and an application processor (AP) having a central processing unit and a master controller for controlling via a common bus a plurality of peripherals including an interface with the signal modulator/demodulator, wherein a memory shared by the modem and the AP is controlled via the interface. The shared memory is preferably an SDRAM. The plurality of peripherals include at least one of an image capture module, a display, and a flash memory.

Preferably, the master controller controls the plurality of peripherals by issuing a packetized command commonly receivable by the plurality of peripherals over the common bus, the packetized command includes a module device select signal used for selecting one of the peripherals, wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt of the packetized command, wherein the packetized command includes a read/write command to a memory shared by the modem and the AP, and data read from the shared memory is sent to the AP with a

strobe signal, the strobe signal is used for strobing the data read into a register in the master controller.

The SDRAM includes a plurality of data banks and an interface for interfacing the master controller. The SDRAM also includes a protection circuit for receiving address data from the AP and the modem and for generating a protect signal upon receiving the same address from the modem and the AP.

According to another embodiment of the present invention, a communication device is provided, comprising: a signal modulator/demodulator having a digital signal processor for effecting radio communications; and an application processor (AP) having a central processing unit and a master controller for controlling via a first bus at least one peripheral and via a second bus a memory shared by the modem and the AP, wherein the master controller further controls via the second bus a flash memory. According to an alternative embodiment, the at least one peripheral is an image capture module.

According to still another embodiment of the present invention, an application processor (AP) for use in a communication device is provided, the application processor comprises: a central processing unit for processing data received from a plurality of peripherals; and a master controller for controlling via a common bus the plurality of peripherals and for interfacing with a signal modulator/demodulator (modem) via the common bus.

Preferably, the communication device further includes a memory, the memory being shared by the modem and the AP, wherein the shared memory is an SDRAM. The plurality of peripherals include at least one of an image capture

module, a display, and a flash memory. The master controller controls the plurality of peripherals by issuing a packetized command commonly receivable by the plurality of peripherals over the common bus, the packetized command includes a module device select signal used for selecting one of the peripherals,

5   wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt of the packetized command.

According to still another aspect of the present invention, an application processor (AP) for use in a communication device is provided, the application processor comprises: a central processing unit for processing data received from

10   a plurality of peripherals; and a master controller for controlling via a first bus the plurality of peripherals and for interfacing with a signal modulator/demodulator (modem) via a second bus.

The communication device further includes a memory, the memory being shared by the modem and the AP, wherein the shared memory is an SDRAM,

15   wherein the plurality of peripherals include at least one of an image capture module, a display, and a flash memory. Preferably, the master controller controls the plurality of peripherals by issuing a packetized command commonly receivable by the plurality of peripherals over the common bus, the packetized command includes a module device select signal used for selecting one of the

20   peripherals.

A method is also provided for controlling a communication device having a signal modulator/demodulator (modem) for effecting radio communications and an application processor (AP) having a central processing unit and a master

6

controller, comprising: controlling via a common bus in the master controller a

plurality of peripherals; and interfacing with the signal modulator/demodulator

(modem) via the common bus, wherein the step of interfacing includes interfacing

a memory shared by the modem and the AP, wherein the step of controlling

5   includes controlling at least one of an image capture module, a display, and a

flash memory and the shared memory is an SDRAM.

Preferably, the step of controlling includes issuing a packetized command

commonly receivable by the plurality of peripherals over the common bus, the

packetized command includes a module device select signal used for selecting

10   one of the peripherals, wherein the selected one of the peripherals returns a

signal to the master controller to acknowledge receipt of the packetized

command.

Brief Description of the Drawings

15

Figure 1 shows a simplified block diagram of a conventional

communication device;

Figure 2 shows a detailed block diagram of the conventional

communication device of Figure 1;

20   Figure 3 shows a block diagram of a communication device according to a

preferred embodiment of the present invention;

Figure 4 shows a block diagram of a bus master controller of Figure 1;

Figure 5 shows a block diagram of a communication device according to

another preferred embodiment of the present invention;

Figure 6 shows a block diagram of a communication device according to another preferred embodiment of the present invention;

Figure 7 shows a definition listing for the signals used by the bus master controller of Figure 4;

Figure 8 shows an illustrative structure of a command packet issued by the bus master controller of Figure 4;

Figure 9 is a definition listing of a command packet field;

Figure 10 shows an illustrative internal register definition of a slave device;

Figure 11 shows a timing diagram of a read operation of data read from a slave device to a bus master controller;

Figure 12 shows a timing diagram of a data write command operation;

Figure 13 shows a structure of a shared memory usable in a communication device according to the present invention;

Figure 14 shows a bank of memories cells of the shared memory with protection circuit; and

Figure 15 shows a timing diagram of read and write operations of a shared memory according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

According to embodiments of the present invention, multiple applications of a mobile communication device are run from the AP chip through a common buss. Control of the multiple applications connected to the common bus can be by a common platform with packetized commands issued by a common master

8

bus controller through the common bus. The common master bus controller replaces the individual interfaces/controllers and their dedicated busses. The AP chip can realize reduced number of pinouts in its chip packaging and therefore the physical size of the AP chip can be reduced. Processing by the CPU using a

5   common platform through a common controller can be reduced, thereby reducing power consumption.   Figure 3 shows a block diagram of a communication device according to a preferred embodiment of the present invention. The illustrative communication device includes two IC chips – an Application Processor chip 310 and a modem chip 350 – and a plurality of application

10   modules disposed external to the two IC chips. The modem chip 350 includes a DSP 395 and modulator/demodulator circuit (not shown) for processing signals to effect wireless or radio communications with other compatible communication devices or base station. The AP chip 310 includes a CPU 311 which controls CPU associated internal functions such as DMA 312, bridge 313 and peripherals

15   314, 315 and 316 . The DMA 312 can access memory devices (including a shared memory 375) for reading and/or writing independently of the CPU 311. The Peripherals 314,315 and 316 can be a timer, a pulse width modulator, USB (Universal Serial Bus) device, I2C device and I2S device.

The CPU 311 operates multiple external applications such as camera

20   module 330, 2D/3D engine 335, display 320, memory module 340, and shared memory 375 through a common bus 305. A bus master controller 380 controls the operations of the external application modules via the common bus 305. A common operating system platform including a common command structure is

9

used. Preferably, the common command is packetized and each command includes a module selector signal to select one of the multiple modules under control. The command and module selection process will be further described below. A shared memory 375 is used for data communication between the modem chip 350 and the AP chip 310. The shared memory can be a dual-port SRAM, controlled by a memory controller (not shown) in the modem chip 350 or the application processor 310.   According to the present embodiment, the shared memory 375 is preferably a synchronous SDRAM, and modem chip 350 uses a bus master controller 390 to control the shared memory 375. The bus master controllers 380 and 390 share a common command structure in communicating with shared memory 375. Interface to the shared memory 375 to/from either the AP chip 310 or the modem chip 350 is the same.

Figure 4 shows a detailed block diagram of a bus master controller usable in the communication device of Figure 3. The bus master controller 380 includes a bus interface 402 for data, control, and signal communication with the CPU. Protocol converter 406 and protocol signal control 410 manages data and control signal flow according to preset protocol. Clock management 404 receives and distributes clock signals for synchronizing the communication device including the external application modules. Address translator 408 receives address data from the CPU and translates the address depending on the application module to be accessed. The translated address is forwarded to packet generator 416, where the address is packetized in a command. The packet generator 416 also receives control signals from protocol signal control 410 for outputting data

pursuant to protocol. Transmit and receive buffer 414 receives data from the CPU through the bus interface 402. A state machine buffer control 412 controls the state and timing of data transmit and receive of transmit and receive buffer 414 pursuant to the preset protocol. Data pack/unpack 418 is used to arrange the data according to specified width of the common data structure. A multiplexer 420 multiplexes address or data signals for outputting through bi-directional bus DIO[n:0]. Data is also read from external application modules through bi-directional bus DIO[n:0]. Protocol signal control 410 sends control signals nCS[x:0], CnD, and nRW and receives control signals RESP and STAT. The data and control signals are transmitted and received through the common bi-directional bus 305.

In operation, the bus master controller 380 acts as the master to control the application modules (slaves) which are connected to the bi-directional bus 305. Centralized commands issued by the master controller are received by the plurality of external slave devices. Control signals output by protocol signal control 410 includes slave select nCS, command CnD, read/write nRW. Data signals are output via DIO[n:0], which can be used to output either data or address signals. The master controller receives at the protocol signal control 410 acknowledged (STAT) and strobe (RESP) signals from a selected one of the plurality of external slave devices for signaling an acknowledgement of receipt of command from master controller 380 and for inputting data through DIO[n:0] under strobe control with strobe signal (RESP). The control and data signals are packetized by packet generator 416.

Figure 7 lists further descriptions of the control signals of the common bus 305. A chip select signal, nCS, is used to select one of the external slave devices connected to common bus 305. Command signal, CnD, is used to signify whether the packet is a command packet or a data packet. Read/write

5   signal, nRW, is used for signaling a read operation or a write operation. This signal is also used to control the direction of data flow on the data line DIO[n:0]. For example, a write operation signals that data is to be written to one of the selected external slave units and the data line DIO is directed outbound from the master controller. When nRW signals a read operation, signal is read from the

10   selected one of the external slaves connected to the common bus 305 and the data lines DIO are directed inbound to be input into master controller 380. The command or data packets are synchronized using the synchronized clock CLK, which is also used to synchronize the external slave units. In a read operation, the selected external slave unit from which data is to be read inputs to the master

15   controller 380 a strobe signal RESP, which is used for strobing the data read from the external slave device into the master controller 380. Upon receipt of a command packet by the selected external slave device, the selected external slave device sends an acknowledged signal, STAT, to the master controller for signaling that it has received the command packet.

20   Figure 8 shows the illustrative command packet structure of commands issued from the bus master controller and Figure 9 shows the descriptions for the command packet field. According to an illustrative embodiment of the present invention, the packet structure is preferably 4-bit wide and the first three locations

12

of the packet 0, 1, 2 are used to specify field definitions and read/write operations. Address or data are included in the packet beginning at location 3. As shown in Figure 9, field R is described as the field specifying the target of the current transaction. The master can access the internal registers of the slave device or the actual data which will be supplied by the slave device. Here, 0 – access normal data; 1 – access the internal register of the slave device. Field TY is the field specifying the type of the current transfer. 00 – Read Transfer; 01 – Reserved; 10 – Write Transfer; 11 – Reserved. Field CL specifies the length of the CMD Packet. 00 – 4 x 4-bit; 01 – 8 x 4-bit; 10-12 x 4-bit and 11-16 x 4-bit. Field DL specifies the size of the Data Packet. Data-Packet Size = $2^{\wedge}DL$ bytes (1, 2 ~ 32,768 bytes). Field A_0 ~ A_i specifies the start address of the requested transfer.

The external slave device selected by master controller 380 responds to the command by raising an acknowledged signal line STAT. The slave device has internal registers which includes mandatory registers or user defined registers. Data from the registers can be read by the master controller by a read command. Data read from the selected external device are strobed into a register (not shown) of master controller 380 from either the rising or falling edges of strobe signal RESP. Figure 10 shows a representative internal register in a slave device and its data map.

Figure 11 is a timing diagram for illustrating a representative read operation of data from a selected application module. As shown, bus master controller issues a clock signal CLK, a high CnD, signaling COMMANDS, and a

13

high transfer signal nRW, signaling a read operation. Application module is selected by nCS (not shown). Commands are sent over the data line DIO[n:0]. As previously described, all control, address, or data signals are sent over the common bus 305. Upon receipt of the commands by the selected external slave

5   device, the slave device sends an active acknowledge signal STAT to the bus master controller. Data is read from the selected external device and placed on data line DIO[n:0], along with strobe signal RESP. The data from data line DIO[n:0] is strobed into the bus master controller 380 using the strobe signals. The bus master controller 380 exercises full control of data transfer operations.

10   For example, the bus master controller 380 can cancel a read operation in progress by issuing a new command or a different transfer command.

Figure 12 is a timing diagram for illustrating a representative write operation of data from the AP chip 310 to a selected application module. As shown, under synchronization by clock signal CLK, bus master controller 380

15   issues command signal CnD and transfer signal nRW. Both command and address information are placed over data lines DIO[n:0] while the transfer signal nRW is held high. The target external application module connected to the common bus 305 is selected by nCS (not shown) and decodes the received commands, which includes the write signal and address data. Pursuant to preset

20   protocol, such as after four command packets, data is sent from the bus master controller 380 over the common bus 305, data lines DIO[n:0] to be read into the internal register of the slave device. The selected slave device signals the receipt of the data packets by raising the acknowledge line STAT.

According to a preferred embodiment of the present invention, the shared memory 375 used for data communication between the AP chip 310 and the modem chip 350 is also controlled by bus master controller 380. Figure 13 shows a shared memory 375 usable in embodiments of the present invention.

5   Shared memory 375 is preferably an SDRAM which includes a plurality of banks of memory cells, bank A, B, C and D. Each bank includes an associated address decoder, protect generator, and bank MUX, to be further described below. The shared memory 375 includes two ports A and B. Port A is connected to the bus master controller 380 of the AP chip 310 through a memory interface and the B

10   port connects to the bus master controller 390 of the modem chip 350 through a second memory interface. Figure 14 shows a more detailed block diagram of banks A and B with associated address decoder, bank MUX, and respective protect generator. The address line is commonly connected to and read by all the associated circuits, e.g., by bank MUX to identify which of the banks A and B

15   memory cells are to be accessed. Each protect generator monitors the address lines of the respective ports A and B and upon detection of the same address at the same bank at both ports A and B, a protect signal NPROT is raised to signal a conflict situation. Memory access is halted during a raised NPROT condition to prevent simultaneous access of the same memory cells.

20   Figure 15 shows a timing diagram of a shared memory access operation according to a preferred embodiment of the present invention. The memory control signals (from memory interfaces A and B) including row address select signal RAS, column select signal CAS, Addresses, Data, and access conflict

signal nProt are shown for Port A and Port B. Also shown are decoded memory access signals from bus master controller 380 of the AP chip 310 and bus master controller 390 of the modem chip 350. The timing diagram shows control signals CnD and nRW are raised to signal memory access, in this case, a read

5   operation, along with packetized commands including addresses of memory to be accessed sent over data lines DIO[n:0] of the common bus 305. Module select signal nCS (not shown) is set at the shared memory 375 as the target application module. Thus, the shared memory 375 is controlled using the same platform, command structure, and through the same common bus 305 as for any

10   other external application module connected to the common bus 305.

The memory interfaces for ports A and B receive the module select signal nCS signifying the shared memory 375 is the selected application module to be accessed. The memory interface A extracts the address information from the packetized commands received from the bus master controllers 380 of the AP

15   chip 310 over the common bus 305. The same process is performed at the bus master controller 390 of the modem chip 350 and memory interface B (not shown). The extracted addresses are received by address decoders of the memory banks, the bank mux, and the protect generators of shared memory 375. Referrring again to Fig. 15, the address information are decoded as row

20   addresses and column addresses. Here, both row address select signals at ports A and B are active (e.g., at low level), and the row address is the same at both ports A and B. Upon encountering the same address RA at both ports A and B, protection generator raises the nProt signal (e.g., high to low transition) at

16

Port B, signaling a memory access conflict to the modem chip 350. The nProt signal at Port B acts to block the modem chip 350 from issuing an acknowledge signal STAT[0] to acknowledge receipt of the memory access command, and holds the strobe signal RESP[0] at inactive level. When RAS signals are no longer present at the same time, or when column address select signals CAS are not present at the same time at port A and port B, protect generator lowers the protection signal nProt, data is read from the shared memory 375. The acknowledge signal STAT[0] is raised at the memory interface B to signal receipt of the access command to the modem chip 350. The data read from the shared memory 375, along with active strobe signals RESP[0] are sent to the modem chip 350. It is preferred that the SDRAM, the protect generator, and interfaces for ports A and B are embedded on a single-chip integrated memory device.

By use of the master-slave, packetized command architecture, multiple applications can be operated via a centralized controller (master) through a common bus. Dedicated interfaces and busses for different application modules are eliminated. The pin count of the AP chip 310 is drastically reduced, thereby reducing the physical size of the AP chip 310. The CPU of the AP chip 310 also realizes reduced process overhead resulting from elimination of the dedicated interfaces/controllers. Further, the use of a common platform at the modem chip 350 facilitates synchronous access of the shared memory 375.

Figure 5 shows another embodiment of the present invention wherein the common bus 305 is replaced by two common busses 305A and 305B. 305A is used for accessing external application modules such as cameras and displays

17

and 305B is used for connecting to external memories such as flash memory and a shared memory. The configuration according to this embodiment facilitates common control of the external application modules other than memories through a common bus, as described above. A separate common bus 305B dedicated for memories allows more flexible memory control, or more memory intensive operations. According to the present embodiment, the shared memory can be a dual-port SDRAM, operated as described above. The shared memory can also be a dual-port SRAM, operated in the conventional manner in communication between the AP chip 310 and the modem chip 350. The use of two common busses also facilitates access of memories such as a flash memory while an external application such as a camera is controlled.

Figure 6 shows still another preferred embodiment according to the present invention, wherein there are two common buses and common bus 305A is used exclusively for a process intensive application, such as a camera module. All other external modules including memory modules and the shared memory are connected to the other common bus 305B. Alternatively, the camera module, along with a flash memory are connected to common bus 305A. In such configuration, common bus 305A is dedicated for camera applications, including transfer of image data directly between the camera module and the flash memory.

Although illustrative embodiments of the present invention have been described herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and

18

that various other changes and modifications may be affected therein by one

skilled in the art without departing from the scope or spirit of the invention.